WHAT IS CLAIMED IS:

1. A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

a first charge storage layer formed on the channel region adjacent the source region;

a second charge storage layer formed on the channel region adjacent the drain region;

a gate insulting layer formed on the channel region between the first and second charge storage layers; and

a gate electrode formed on the gate insulating layer and the first and second charge storage layers.

2. The memory cell as recited in claim 1, wherein the first and second charge storage layers each include a tunnel oxide layer, a charge trapping layer and a blocking insulating layer in a stacked formation.

3. The memory cell as recited in claim 1, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the first and second charge storage layers.

4. The memory cell as recited in claim 1, wherein the gate insulating layer comprises sidewalls that are aligned with sidewalls of the first and second charge storage layers.

5. The memory cell as recited in claim 1, wherein the gate electrode comprises:

a gate pattern formed on the gate insulating layer; and

a gate sidewall pattern formed on each of the first and second charge storage layers.

6. A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region;

a gate insulting layer formed on the channel region between the at least two charge storage layers;

a gate pattern formed on the gate insulting layer;

at least one lower sidewall pattern formed on at least one of the at least two charge storage layers; and

at least one upper sidewall pattern formed on the at least one lower sidewall pattern,

wherein the at least one upper sidewall pattern electrically contacts the at least one lower sidewall pattern and the gate pattern.

7. The memory cell as recited in claim 6, wherein the at least two charge storage layers each include a tunnel oxide layer, a charge trapping layer and a blocking insulting layer.

8. The memory cell as recited in claim 6, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the at least two charge storage layers.

9. The memory cell as recited in claim 6, wherein the gate insulating layer comprises sidewalls that are aligned with sidewalls of the at least two charge storage layers.

10. A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first

position is adjacent the source region and the second position is adjacent the drain region;

a gate insulting layer formed on the channel region between the at least two charge storage layers;

a gate pattern formed on the gate insulting layer;

at least one lower sidewall pattern formed on at least one of the at least two charge storage layers; and

at least one upper sidewall pattern formed on the at least one lower sidewall pattern,

wherein the at least one lower sidewall pattern is electrically insulated from the at least one upper sidewall pattern and the gate pattern.

11. The memory cell as recited in claim 10, wherein the at least two charge storage layers each include a tunnel oxide layer, a charge trapping layer and a blocking insulting layer.

12. The memory cell as recited in claim 10, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the at least two charge storage layers.

13. The memory cell as recited in claim 10, further comprising at least one inter-gate insulating layer interposed between the at least one lower sidewall pattern and the at least one upper sidewall pattern.

14. The memory cell as recited in claim 10, wherein the gate

insulating layer comprises sidewalls aligned with sidewalls of the at least two charge storage layers.

15. The memory cell as recited in claim 10, wherein a voltage is independently applied to the gate pattern and to the at least one lower sidewall pattern.

16. A method for fabricating a memory cell, comprising:

stacking an insulating layer, a lower conductive layer and a mask layer on a semiconductor substrate;

patterning the mask layer, the lower conductive layer and the insulating layer to form a gap region;

forming a gate oxide layer on exposed surfaces of the semiconductor substrate and the lower conductive layer in the gap region;

forming a gate pattern on the gate oxide layer for filling the gap region;

removing the mask layer to expose sidewall portions of the gate pattern;

forming an upper sidewall pattern on each exposed sidewall portion of the gate pattern;

patterning the lower conductive layer and the insulating layer to form a lower sidewall pattern and a charge storage layer under each upper sidewall pattern, wherein the gate pattern and each upper sidewall pattern is used as an etching mask; and

forming a source region and a drain region in the semiconductor

substrate adjacent a first charge storage layer and a second charge storage layer, respectively, wherein the gate pattern and each upper sidewall pattern is used as an etching mask.

17. The method as recited in claim 16, further comprising doping impurities into an exposed portion of the semiconductor substrate in the gap region to form a channel region.

18. The method as recited in claim 16, wherein forming the upper sidewall pattern on each exposed sidewall portion comprises:

forming an upper conductive layer on the semiconductor substrate; and

anisotropically etching the upper conductive layer to expose the lower conductive layer.

19. A method for fabricating a memory cell, comprising:

stacking an insulating layer, a lower conductive layer, an interlayer insulating layer and a mask layer on a semiconductor substrate;

patterning the mask layer, the interlayer insulating layer, the lower conductive layer and the insulating layer to form a gap region;

forming a gate oxide layer on exposed surfaces of the semiconductor substrate and the lower conductive layer in the gap region;

forming a gate pattern on the gate oxide layer for filling the gap region;

removing the mask layer to expose the interlayer insulating layer and

sidewall portions of the gate pattern;

forming an upper sidewall pattern on each exposed sidewall portion of the gate pattern and on the interlayer insulting layer;

patterning the interlayer insulating layer, the lower conductive layer and the insulating layer to form an inter-gate insulating layer, a lower sidewall pattern and a charge storage layer under each upper sidewall pattern, wherein the gate pattern and each upper sidewall pattern is used as an etching mask; and

forming a source region and a drain region in the semiconductor substrate adjacent a first charge storage layer and a second charge storage layer, respectively, wherein the gate pattern and each upper sidewall pattern is used as an ion implantation mask.

20. The method as recited in claim 19, further comprising doping impurities into an exposed portion of the semiconductor substrate in the gap region to form a channel region.

21. The method as recited in claim 19, wherein forming the upper sidewall pattern on each exposed sidewall portion comprises:

forming an upper conductive layer on the semiconductor substrate after removing the mask layer; and

anisotropically etching the upper conductive layer to expose the interlayer insulting layer.